REMARKS/ARGUMENTS

Applicants acknowledge receipt of the Office action dated June 29, 2005, in which the Examiner: 1) rejected claims 13, 17 and 19-22 as allegedly indefinite; 2) rejected claims 1-4, 8, 15 and 19 as allegedly anticipated by Morrison (U.S. Pat. No. 6,625,679); and 3) objected to claims 5-7, 9-12, 14 and 16 as dependent on a rejected base claim, but otherwise allowable.

With this Response, Applicants amend claims 5, 9, 14, 16-17 and 19-20, and cancels claim 15. Reconsideration is respectfully requested.

I. SECTION 112 REJECTIONS

Claims 13, 17 and 19-22 stand rejected as allegedly indefinite. With regard to claim 13, the Office action alleges that there is insufficient antecedent basis for the limitation "the port logic." Applicants respectfully traverse this assertion, as the antecedent basis for the term "the port logic" is within claim 13, stating, "wherein each processor further comprises a port logic."

With regard to claim 21, the Office action alleges that there is insufficient antecedent basis for the limitation "the means for storing." Applicants respectfully traverse this rejection, as the antecedent basis for the term "the means for storing" is within claim 19 (from which claim 21 depends), claim 19 stating, "a plurality of means for executing programs and instructions coupled to each other, each of the plurality of means for executing coupled to **a means for storing data** and instructions local each of the plurality of means for executing... ."

Applicants amend claims 17 and 19 to address the rejections with respect to these claims.

II. EFFECTIVELY ALLOWED CLAIMS

The Office action objects to claims 5-7, 9-12, 14 and 16 as dependent on a rejected base claim, but otherwise allowable. With this Response, Applicants rewrite claims 5, 9, 14 and 16 into independent form, including the limitation of their base claims and intervening claims (if any).

Applicants further submit that claim 13 (which depends from claim 9), should also be in a condition for allowance as it does not suffer from indefiniteness as discussed above.

The only rejection lodged against claim 17 was the Section 112 rejection. With the Response, Applicants not only amend claim 17 to address the Section 112 rejection, but also to rewrite claim 17 into independent form.

The only rejection lodged against claims 20 and 22 was the Section 112 rejection based on dependency from claim 19. With the Response, Applicants rewrite claim 20 into independent form, and simultaneously address the Section 112 rejection. As discussed above, the Section 112 rejection of claim 21, which depends from claim 20, is without merit.

Thus, claims 5-7, 9-14, 16-18 and 20-22 should be in a condition for allowance.

III. ART-BASED REJECTIONS

The Office action dated June 29, 2005 rejects claims 1-4, 8 and 19 as allegedly anticipated by Morrison.

Morrison is directed to an apparatus and method for converting interrupt transactions to interrupt signals to distribute interrupts to IA-32 processors. (Morrison Title). The Office action cites Morrison Column 8, lines 26-46. This portion of Morrison is reproduced below for convenience of the discussion:

> An interrupt handler may assume that the occurrence of the interrupt implies that the associated DMA is complete, while, in reality, the data available to the processor is stale. Interrupt handlers for PCI devices do not have this problem since the PCI specification requires the ISR to perform a read on the interrupting device which forces all pending DMA transfers to be completed. Interrupt handlers for other peripheral buses (e.g., ISA buses) do not require any special action to be performed by the handler to force pending DMA transfers to complete prior to acting on the interrupt.
>
> To avoid this situation, the bridge 112_i guarantees that system bus transactions are complete that were pending prior to the original interrupt transaction on the system.
>
> **The above solution to the ISA DMA problem in the bridge 112_i has an implication for the interrupt forwarding algorithm. To insure the dependencies are correctly resolved, the bridge 112_i selects the highest priority interrupt from all interrupts that have had all pending coherency traffic flushed that were pending at the time the original interrupt transaction 210 was received.**

(Morrison Col. 8, lines 26-46 (emphasis added)). The clear implication of the cited section, and Morrison in general, appears to be that the bridge 112 only forwards an interrupt (from an I/O device indicating that a DMA is complete as far as the I/O device is concerned) to the processor when all the coherency traffic pending when the interrupt was asserted has been flushed.

Claim 1, by contrast, specifically recites, "periodically stalling issuance of input/output (I/O) device accesses by a program in a multiple-processor computer system; and during the stalling step completing pending I/O device reads." As Applicants understand Morrison, the processors of Morrison are allowed to continue execution, and are only interrupted (sent the interrupt by the bridge device) once coherency traffic has been flushed. This teaching appears diametrically opposed to "periodically stalling issuance of input/output (I/O) device accesses by a program in a multiple-processor computer system; **and during the stalling** step completing pending I/O device reads."

Claim 8 specifically recites, "a plurality of processors coupled to each other; at least one of the plurality of processors coupled to an input/output (I/O) device by way of a bridge logic device; and wherein each of the plurality of processors periodically executes a program that operates to cease issuance of I/O device writes until pending I/O device reads complete." Again, as Applicants understand Morrison, the processors of Morrison are allowed to continue execution, and are only interrupted (sent the interrupt by the bridge device) once coherency traffic has been flushed. This teaching appears diametrically opposed to "wherein each of the plurality of processors periodically executes a program that operates to cease issuance of I/O device writes until pending I/O device reads complete."

Based on the foregoing, Applicants respectfully submits that claims 1-4, 8 and 19 are not taught, expressly or impliedly, by Morrison, and thus these claims should be in a condition for allowance.

IV. CLAIM CANCELLATIONS

With this Response, Applicants cancel claim 15 without prejudice to later assert the claim, such as in a continuation application.

V. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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